1. A method to reduce switching noise on an integrated circuit device, said method comprising:

providing an integrated circuit device comprising an upper voltage node, a ground, and a plurality of switchable capacitors wherein each said switchable capacitor is connected from said upper voltage node to said ground;

tracking an operating mode of said integrated circuit device;

selecting an optimal capacitance value based on said operating mode; and

selecting a set of said switchable capacitors from said plurality of switchable capacitors to thereby connect said optimal capacitance value from said upper voltage node to said ground.

2. The method according to Claim 1 wherein said step of selecting an optimal capacitance value based on said operating mode is by a method further comprising:

determining a proportion of total circuits in said integrated circuit device that are switching in said operating mode; and

calculating said optimal capacitance value based on said proportion.

3. The method according to Claim 2 wherein said optimal capacitance value is calculated using a formula based on capacitance loading in switching circuits and capacitance loading in non-switching circuits.

4. The method according to Claim 1 wherein said operating mode comprises a power-saving mode.

5. The method according to Claim 1 wherein said switchable capacitors each comprise a capacitor and a switch connected in series.

6. The method according to Claim 5 wherein said capacitor comprises an MOS device.

7. The method according to Claim 5 wherein said capacitor is connected to said upper voltage node and said switch is connected to said ground.

8. The method according to Claim 5 wherein said capacitor is connected to said ground and said switch is connected to said upper voltage node.

9. The method according to Claim 5 wherein said switch comprises an MOS transistor.

10. The method according to Claim 1 wherein said switchable capacitors each comprise:

a PMOS transistor having source, drain, and gate terminals wherein said source terminal is coupled to said upper voltage node;

an NMOS transistor having source, drain, and gate terminals wherein said source terminal is coupled to said ground, wherein said drain terminal is coupled to said PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS transistor drain terminal;

a first switch coupled between said PMOS transistor gate terminal and said upper voltage node; and

a second switch coupled between said NMOS transistor gate terminal and said ground.

11. The method according to Claim 10 wherein said first and second switches comprise MOS transistors.

12. A method to reduce switching noise on an integrated circuit device, said method comprising:

providing an integrated circuit device comprising an upper voltage node, a ground, and a plurality of switchable capacitors wherein each said switchable capacitor is connected from said upper voltage node to said ground and wherein said switchable capacitors each comprise a capacitor and a switch connected in series;

tracking the operating mode of said integrated circuit device;

selecting an optimal capacitance value based on said operating mode by a method comprising:

determining a proportion of total circuits in said integrated circuit device that are switching in said operating mode; and

calculating said optimal capacitance value based on said proportion; and

selecting a set of said switchable capacitors from said plurality of switchable capacitors to thereby connect said optimal capacitance value from said upper voltage node to said ground.

13. The method according to Claim 12 wherein said optimal capacitance value is calculated using a formula based on capacitance loading in switching circuits and capacitance loading in non-switching circuits.

14. The method according to Claim 12 wherein said operating mode comprises a power-saving mode.

15. The method according to Claim 12 wherein said capacitor comprises an MOS device.

16. The method according to Claim 12 wherein said capacitor is connected to said upper voltage node and said switch is connected to said ground.

17. The method according to Claim 12 wherein said capacitor is connected to said ground and said switch is connected to said upper voltage node.

18. The method according to Claim 12 wherein said switch comprises an MOS transistor.

19. An integrated circuit device comprising:

an upper voltage node;

a ground;

a plurality of switchable capacitors wherein each said switchable capacitor is connected from said upper voltage node to said ground;

a means of tracking the operating mode of said integrated circuit device;

a means of selecting an optimal capacitance value based on said operating mode; and

a means of selecting a set of said switchable capacitors from said plurality of switchable capacitors to thereby connect said optimal capacitance value from said upper voltage node to said ground.

20. The device according to Claim 19 wherein said means of selecting an optimal capacitance value based on said operating mode comprises:

a means of determining a proportion of total circuits in said integrated circuit device that are switching in said operating mode; and

a means of calculating said optimal capacitance value based on said proportion.

21. The device according to Claim 20 wherein said optimal capacitance value is calculated using a formula based on capacitance loading in switching circuits and capacitance loading in non-switching circuits.

22. The device according to Claim 19 wherein said

operating mode comprises a power-saving mode.

23. The device according to Claim 19 wherein said switchable capacitors each comprise a capacitor and a switch connected in series.

24. The device according to Claim 23 wherein said capacitor comprises an MOS device.

25. The device according to Claim 23 wherein said capacitor is connected to said upper voltage node and said switch is connected to said ground.

26. The device according to Claim 23 wherein said capacitor is connected to said ground and said switch is connected to said upper voltage node.

27. The device according to Claim 23 wherein said switch comprises an MOS transistor.

28. The device according to Claim 19 wherein said switchable capacitors each comprise:

a PMOS transistor having source, drain, and gate terminals wherein said source terminal is coupled to said

upper voltage node;

an NMOS transistor having source, drain, and gate terminals wherein said source terminal is coupled to said ground, wherein said drain terminal is coupled to said PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS transistor drain terminal;

a first switch coupled between said PMOS transistor gate terminal and said upper voltage node; and

a second switch coupled between said NMOS transistor gate terminal and said ground.

29. The device according to Claim 28 wherein said first and second switches comprise MOS transistors.

30. The device according to Claim 28 wherein said first and second switches are controlled by a single signal.